SCOPE

Senior Consulting Program for Engineering

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The Correspondence Algorithm

Algorithm Selection

Rank Transform Algorithm

126	127	129
125	128	130
127	129	130

→

	X	

Number of red boxes = 4

Census Algorithm

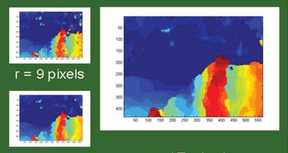
126	127	129
125	128	130
127	129	130

→

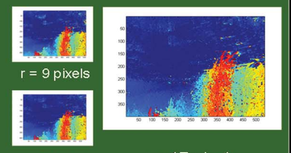
1	1	0
1	X	0
1	0	0

11010100

Rank Transform Results

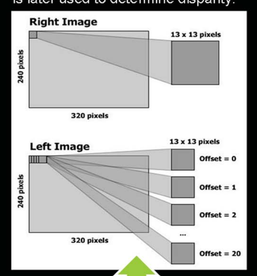


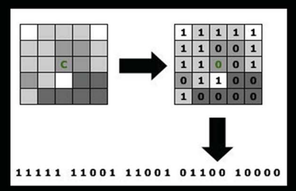
Census Results



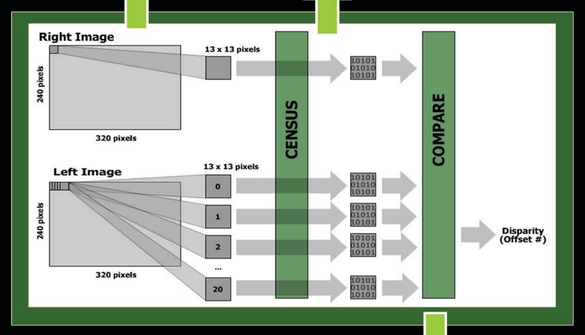
Algorithm Implementation

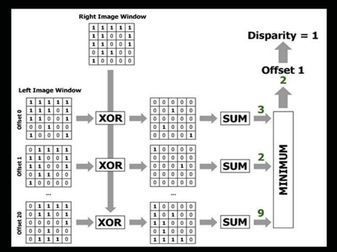
Comparison of Right Image window with Left Image windows, to find which is the best match. The offset of the best match is later used to determine disparity.





This is how these comparisons are actually made; bit strings are obtained for each window, based on the relationship of surrounding pixels to the center pixel.





Once the bit strings from the right window and left windows are obtained, they are compared using XOR. This gives us the number of differences between the strings.

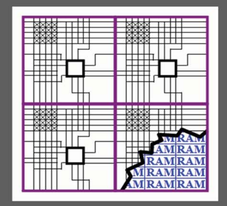
The pair of windows with the fewest differences is the best match and its offset is the disparity.

Project Vision

- Stereo Vision Platform
  - Basis for agricultural applications

- Low Cost
  - Less than $1K

- Embedded
  - Without Laptop, CPU



- Compliments Existing Technology
  - Starfire GPS Navigation

Stereo Vision Implementation

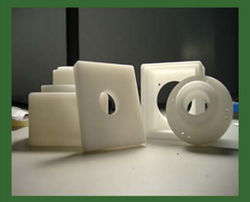
Image Acquisition: Cameras

- OV3620
  - cell phone
- OV7710
  - Automotive
  - 320 x 240
  - ¼" sensor
  - Anti-blooming
  - Exposure control
  - White balance
- *SCCB* : Complex state machine implementation

OmniVision 7710
30fps @ 24.57MHz Clock
(320x240)

Camera Housing

- Modeled in Solidworks
- SLA Rapid Prototyping
- High Res ABS-like plastic



PIC – 18F2550

- Used for SCCB
- RISC Microcontroller
- C Compiler
- Price, ~$5

USB

Digilent Extender Board

- Not designed for Hi-Speed applications

Quick USB

- Higher speed
- Designed for easy integration with existing systems

Software

C++ DLL captures data from FPGA

- Gets most recent complete data set
- Delivers left camera image, disparity image

Python script displays, stores data

- Images update as fast as PC allows
- Can store images on host PC

Time stamping

Xilinx Spartan III FPGA

- Up to 1.6M system gates
- From 66 to 784 I/Os
- Embedded 18x18 Multipliers
- Xilinx Spartan III: $12/million gates
- Optimized for low cost consumer applications

Scalability

Image Edge Considerations Ignored

Cheetah Generator

- Creates Verilog files for Algorithm
- Contains Templates to Adapt Algorithm for Scalability (Maximum Disparity, Window Size, Image Width)

Multiple FPGA solution

- Perform the Census Transform on multiple smaller FPGAs
- Have a larger FPGA perform correspondence

System Pricing

Current Platform

- Quick USB, ~$150
- Camera development kit, ~$200 ea.
- New horizons FPGA board, ~$450
- Cables, proto-boards, etc. ~$100

Large Quantity

- Cameras $15 (Qty 10K)
- FPGAs $50 (Lg. Qty)
- USB Cypress Chip $8 (Qty 1K)

Similar Products

Videre Stereo on a Chip
- 30 fps @ 640x480, ~$1,400

Point Grey Bumblebee
- 30 fps @ 640 x 480, ~$1,995

Tyzx Deep Sea
- 30 fps @ 512 x 480, ~$10,000

Timeline, Next Steps

SCOPE '05-'06
- Explored existing stereovision options
- Identified and tested algorithms
- Programmed algorithm on FPGA
- Obtained, interpreted, and provided camera data through USB

SCOPE '06-'07
- Refinement of algorithm
- Calculate distance from disparity
- Optics optimization (lens, registration)
- Technology demonstration

SCOPE '07-'08
- Integration of multiple camera pairs
- Technology transfer